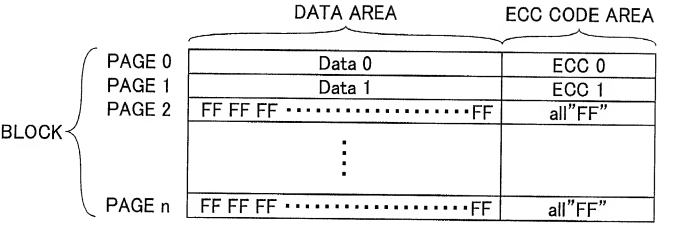
TOSHIBA SCETT660

FIG.1



TOSHIBA SEMICONDUCTOR

FIG.2

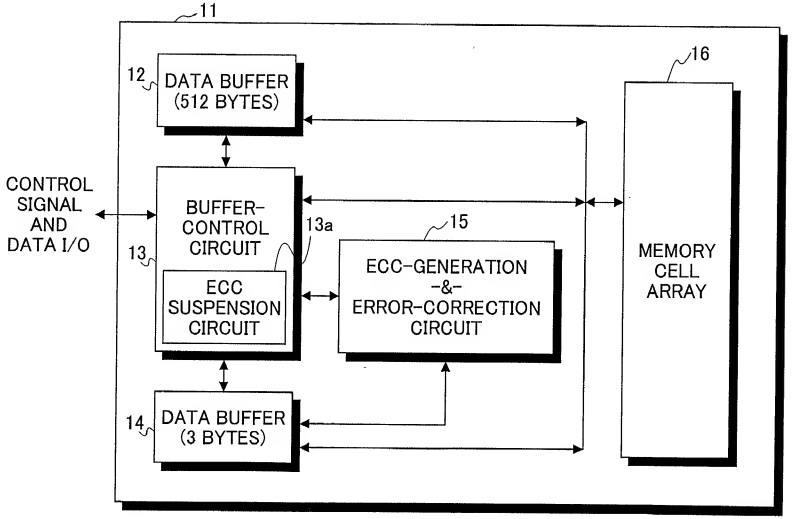


FIG.3

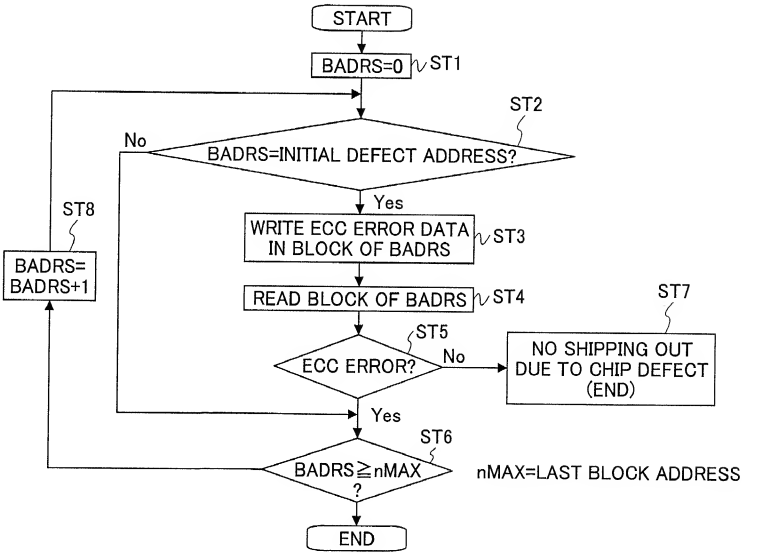

START
BADRS=0
ST1
ST2
No
BADRS=INITIAL DEFECT ADDRESS?
Yes
ST8
WRITE ECC ERROR DATA IN BLOCK OF BADRS
ST3
BADRS= BADRS+1
READ BLOCK OF BADRS
ST4
ST7
ST5
ECC ERROR?
No
NO SHIPPING OUT DUE TO CHIP DEFECT (END)
Yes
ST6
BADRS≧nMAX ?
nMAX=LAST BLOCK ADDRESS
END

FIG.4

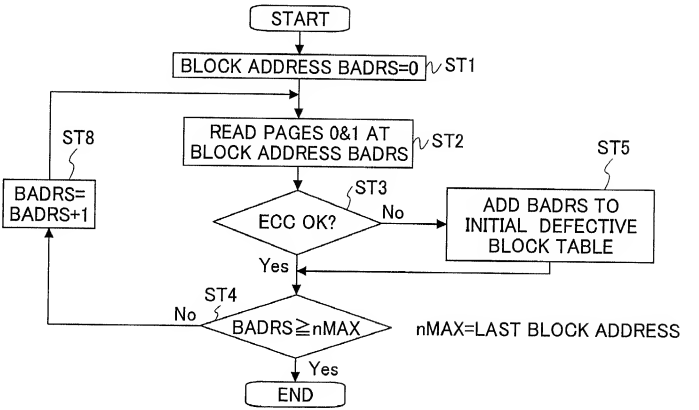

START
BLOCK ADDRESS BADRS=0
ST1
READ PAGES 0&1 AT BLOCK ADDRESS BADRS
ST2
ECC OK?
ST3
No
ADD BADRS TO INITIAL DEFECTIVE BLOCK TABLE
ST5
Yes
BADRS≧nMAX
ST4
No
Yes
nMAX=LAST BLOCK ADDRESS
BADRS= BADRS+1
ST8
END

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FIG.5

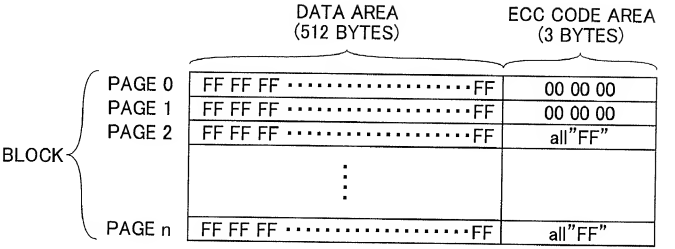
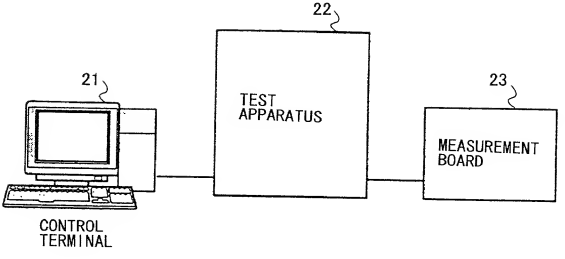


FIG.6

	STATUS	DESCRIPTION
I/O0	PROGRAM/ERASE	0=SUCCESS, 1=FAILURE
I/O1	ECC ERROR DETECTION	0=NO ERROR, 1=ERROR DETECTED
I/O2	ECC ERROR CORRECTION	0=NO DATA CORRECTION, 1=DATA CORRECTED
I/O3	ECC ERROR CORRECTION	RESERVED
I/O4	ECC ERROR CORRECTION	RESERVED
I/O5	ECC ERROR CORRECTION	RESERVED
I/O6	READY/BUSY	0=BUSY, 1=READY
I/O7	WRITE PROTECTION	0=PROTECTED, 1=NOT PROTECTED

FIG. 7


22
21
23
TEST
APPARATUS
MEASUREMENT
BOARD
CONTROL
TERMINAL